

High Voltage Thyristor Module

$$V_{RRM} = 2 \times 2200 \text{ V}$$

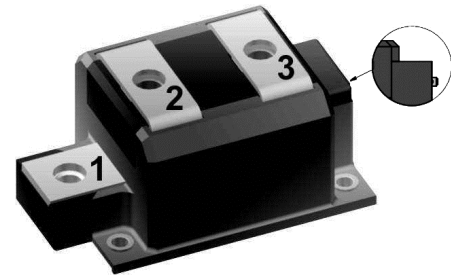
$$I_{TAV} = 650 \text{ A}$$

$$V_T = 1.16 \text{ V}$$

Phase leg

Part number

MCNA650P2200CA



Backside: isolated

 E72873



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Direct Copper Bonded Al₂O₃-ceramic

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: ComPack

- Isolation Voltage: 4800 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Base plate: Copper internally DCB isolated
- Advanced power cycling
- Phase Change Material available

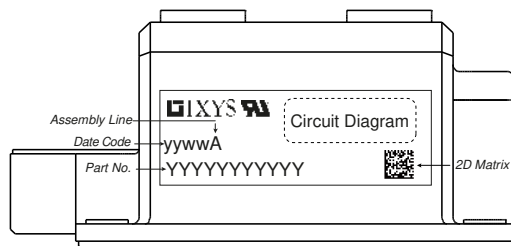
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Rectifier			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			2300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			2200	V
I_{RD}	reverse current, drain current	$V_{R/D} = 2200 V$	$T_{VJ} = 25^{\circ}C$		2	mA
		$V_{R/D} = 2200 V$	$T_{VJ} = 125^{\circ}C$		40	mA
V_T	forward voltage drop	$I_T = 650 A$	$T_{VJ} = 25^{\circ}C$		1.19	V
		$I_T = 1300 A$			1.53	V
		$I_T = 650 A$	$T_{VJ} = 125^{\circ}C$		1.16	V
		$I_T = 1300 A$			1.59	V
I_{TAV}	average forward current	$T_C = 85^{\circ}C$	$T_{VJ} = 140^{\circ}C$		650	A
$I_{T(RMS)}$	RMS forward current	180° sine			1020	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 140^{\circ}C$		0.75	V
r_T	slope resistance				0.63	mΩ
R_{thJC}	thermal resistance junction to case				0.045	K/W
R_{thCH}	thermal resistance case to heatsink			0.02		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}C$		2555	W
I_{TSM}	max. forward surge current	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		16.0	kA
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		17.3	kA
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 140^{\circ}C$		13.6	kA
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		14.7	kA
I^2t	value for fusing	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		1.28	MA ² s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		1.24	MA ² s
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 140^{\circ}C$		924.8	kA ² s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		897.7	kA ² s
C_J	junction capacitance	$V_R = 700 V \quad f = 1 \text{ MHz}$	$T_{VJ} = 25^{\circ}C$		469	pF
P_{GM}	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 140^{\circ}C$		120	W
		$t_p = 300 \mu s$			60	W
P_{GAV}	average gate power dissipation				30	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 140^{\circ}C; f = 50 \text{ Hz}$	repetitive, $I_T = 1950 A$		100	A/μs
		$t_p = 200 \mu s; di_G/dt = 1 A/\mu s;$	non-repet., $I_T = 650 A$		500	A/μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$	$T_{VJ} = 140^{\circ}C$		1000	V/μs
		$R_{GK} = \infty; \text{method 1 (linear voltage rise)}$				
V_{GT}	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		2	V
			$T_{VJ} = -40^{\circ}C$		3	V
I_{GT}	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		300	mA
			$T_{VJ} = -40^{\circ}C$		400	mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 140^{\circ}C$		0.25	V
I_{GD}	gate non-trigger current				10	mA
I_L	latching current	$t_p = 30 \mu s$	$T_{VJ} = 25^{\circ}C$		400	mA
		$I_G = 1 A; di_G/dt = 1 A/\mu s$				
I_H	holding current	$V_D = 6 V \quad R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		300	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	μs
		$I_G = 1 A; di_G/dt = 1 A/\mu s$				
t_q	turn-off time	$V_R = 100 V; I_T = 650 A; V = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^{\circ}C$		350	μs
		$di/dt = 10 A/\mu s \quad dv/dt = 50 V/\mu s \quad t_p = 200 \mu s$				

Package ComPack		Ratings				
Symbol	Definition	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal			1200	A
T_{VJ}	virtual junction temperature		-40		140	°C
T_{op}	operation temperature		-40		125	°C
T_{stg}	storage temperature		-40		125	°C
Weight				500		g
M_D	mounting torque		3		5	Nm
M_T	terminal torque		12		14	Nm
$d_{Spp/App}$	creepage distance on surface striking distance through air	terminal to terminal	21.0			mm
$d_{Spb/Apb}$		terminal to backside	18.0			mm
V_{ISOL}	isolation voltage	t = 1 second	4800			V
		t = 1 minute	4000			V

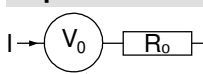

Part description

M = Module
 C = Thyristor (SCR)
 N = High Voltage Thyristor
 A = (>= 2000V)
 650 = Current Rating [A]
 P = Phase leg
 2200 = Reverse Voltage [V]
 CA = ComPack

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	MCNA650P2200CA	MCNA650P2200CA	Box	3	523321

Equivalent Circuits for Simulation

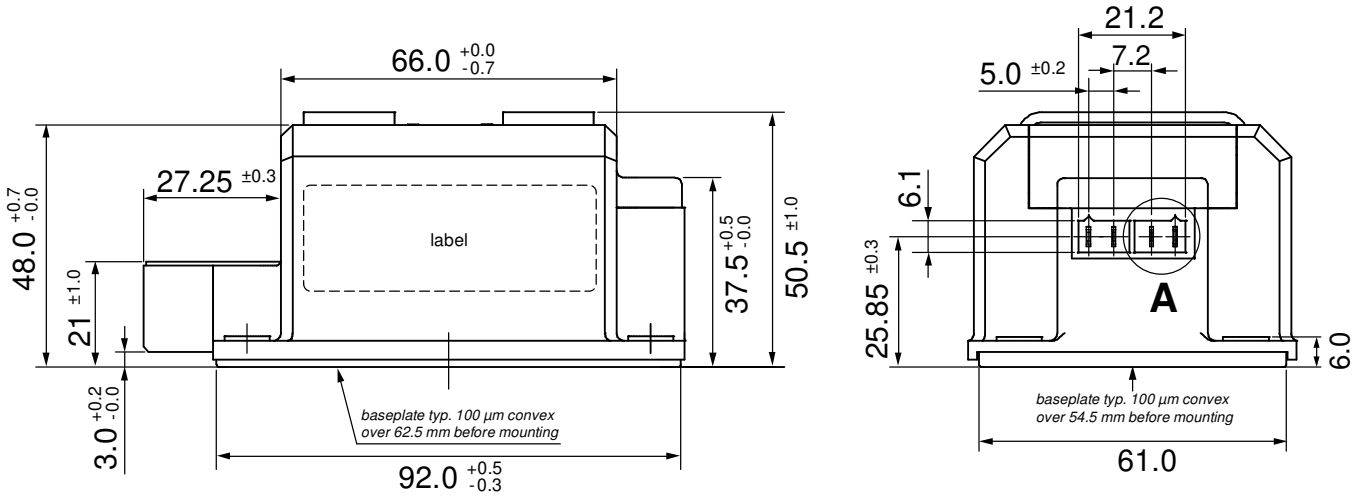
* on die level

 $T_{VJ} = 140^{\circ}\text{C}$

Thyristor

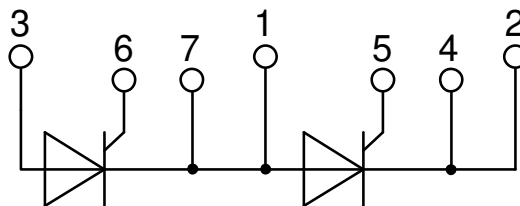
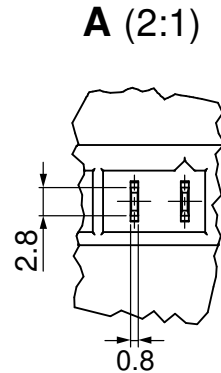
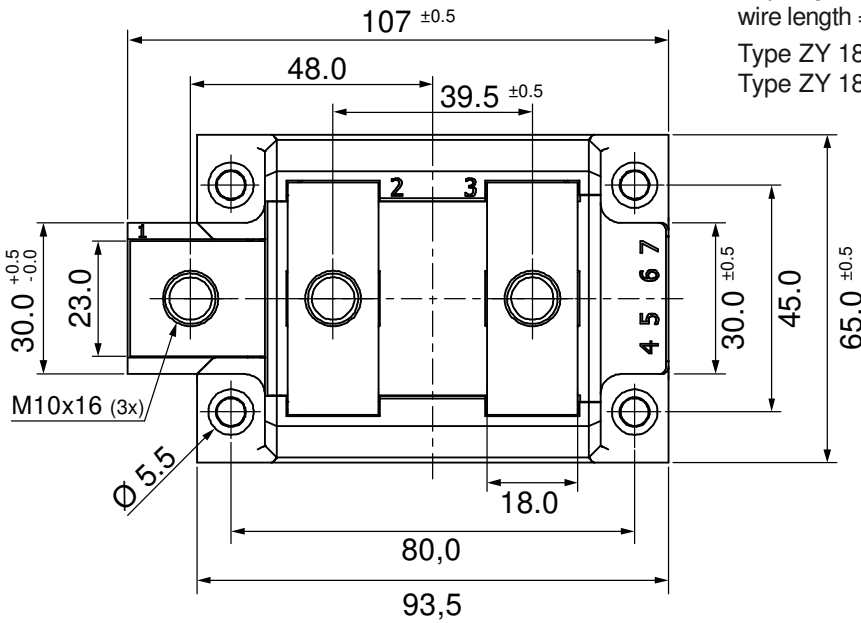
$V_{0\ max}$	threshold voltage	0.75	V
$R_{0\ max}$	slope resistance *	0.44	mΩ



Outlines ComPack



Optional accessories for modules
 Keyed gate/cathode twin plugs with
 wire length = 350 mm, gate = white, cathode = red
 Type ZY 180L (L = Left for pin pair 4/5) } UL 758,
 Type ZY 180R (R = Right for pin pair 6/7) } style 3751



Thyristor

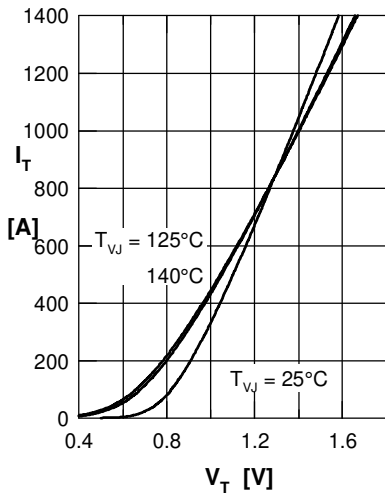


Fig. 1 Forward characteristics

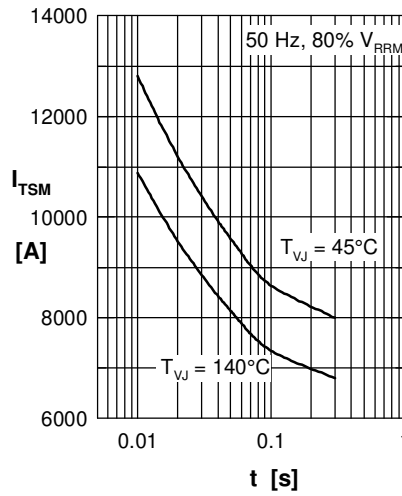


Fig. 2 Surge overload current
 I_{TSM} : crest value, t : duration

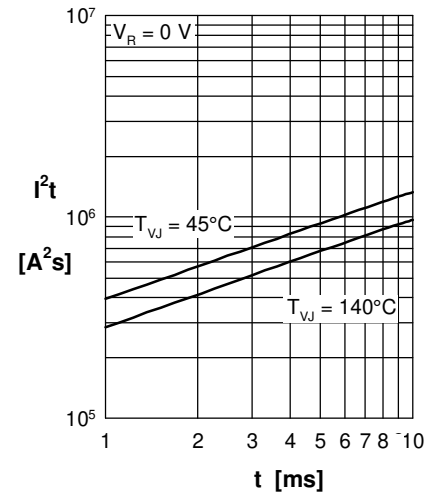


Fig. 3 I^2t versus time (1-10 s)

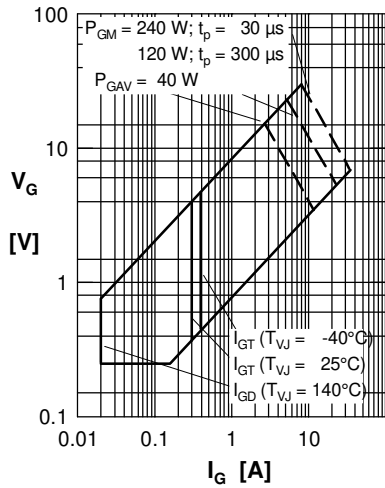


Fig. 4 Gate voltage & gate current

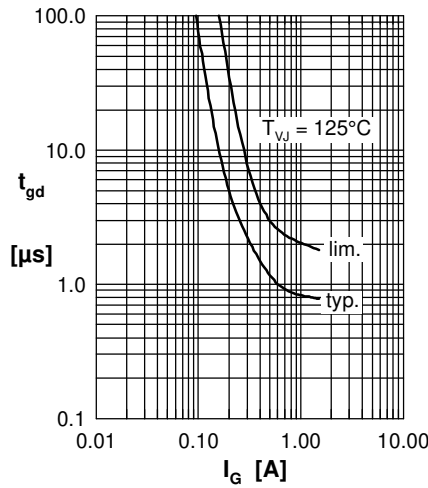


Fig. 5 Gate controlled delay time t_{gd}

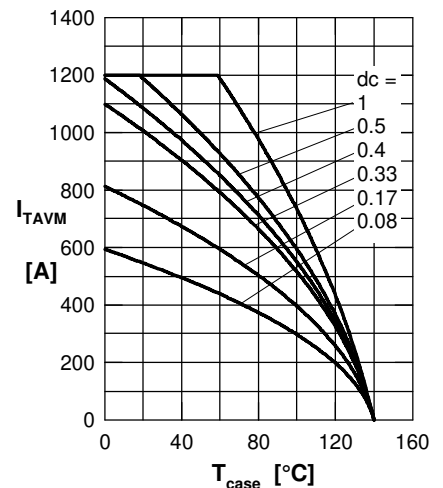


Fig. 6 Max. forward current at case temperature

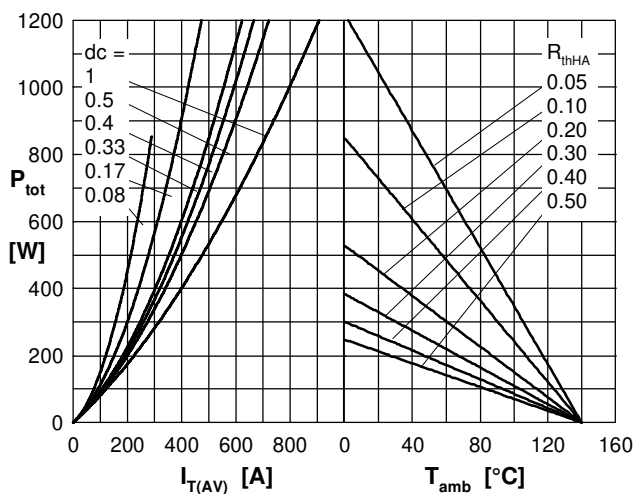


Fig. 7a Power dissipation versus direct output current
 Fig. 7b and ambient temperature

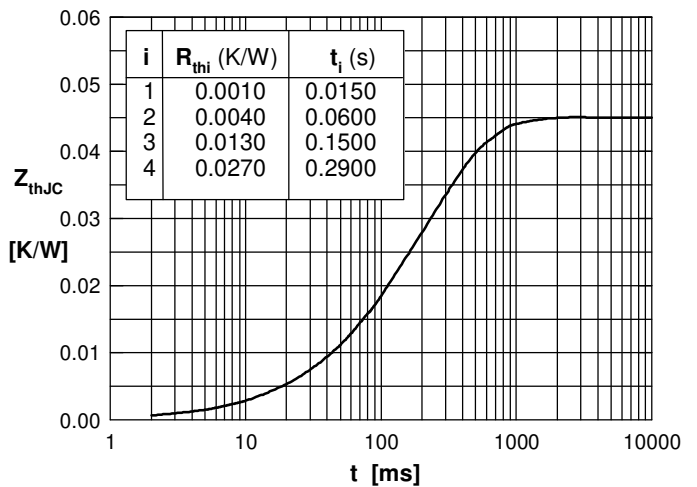


Fig. 8 Transient thermal impedance junction to case